Innovative: International Multi-disciplinary Journal of Applied Technology
(ISSN 2995-486X) VOLUME 02 ISSUE 10, 2024

# Analytical Study of Turbo Code with Orthogonal Frequency Division Multiplexing Based on FPGA for Wireless Communication System

**Maryam Salim Ali**
Computer Engineering Department, Al_Shatrah University, Thi_Qar, Iraq

**Hawraa Abdulelah Kadhum**
Mechatronic engineering Department, Al-Muthanna University, Al-Muthanna, Iraq

**Ahmed Butti**
Computer Engineering Techniques Department, Imam Ja'afar Al_Sadiq University, Thi_Qar, Iraq

**Abstract:**

Dealing with many of users simultaneously and error free communication with maximum utilization of limited spectrum, improved bit error rate (BER) has become very important. Turbo code provides modest decoding complexity for large block length and better bit error rate as compared with other codes. The main part of a turbo code is convolution code. It is one of the best types of the channel coding to increase the data transmission rate at a fixed error rate or error rate could be reduced with a fixed data transmission rate in digital communication systems. One of the most modern parts of a wireless system is the Orthogonal Frequency Division Multiplexing (OFDM), which is one of the multiple modulation systems. The main aim of this work is to study the design and synthesis turbo code with OFDM system. Simulation performance of OFDM design in this paper showed successfully result, which composed of the main parts Serial / Parallel, 8QAM, 16IFFT. System implementation has been done using FPGA technology with Altera Cyclone II boards.

**Keywords:** Orthogonal Frequency Division Multiplexing; Turbo code; FPGA; Data transmission rate; Digital communication system.

## 1. Introduction

In digital communication systems to improve the value of output data, channel coding is used. It contracts with several numbers of methods that are being utilized for the development of the performance of our communication system. It develops the information transfer rate at a stable error

rate or error rate can be miniature with a fixed information transfer rate. The maximum of the information transfer shows the digital communication systems are controlled by Shannon limit [1]. Forward Error Correction (FEC) and Automatic Repeat Request (ARQ) are two basic errors correcting orders which have been used in communication systems. The choice of these orders is application subordinate.

FEC is a progressive technique for error regulator during data transmission, whereby dismissed information is added to the original data, which permits the receiver to detect and correct errors deprived of the requirement to resend the data. The main benefit of FEC is to escape the retransmission, at the cost of greater bandwidth requirements and later is employed in the states where retransmission is moderately costly or impracticable [2].

Turbo codes are a kind of high execution FEC codes, which were the first feasible codes to carefully process the channel ability, a theoretical maximum for the code rate at which consistent communication is yet possible to give a fixed noise scale. Turbo codes can be used in satellite communications and other applications where designers request to check credible information transfer over bandwidth or passivity-controlled communication links in the entity of data corrupting noise. Turbo codes can be executed by designing the Turbo Encoder and Decoder by Viterbi algorithm [3].

According to the characteristic delay in the procedures of equalization and coding and the hardware high cost, using these methods in working systems at high bit rates is quite difficult. New modulation methods are being executed to save up with the need more communication capacity, Orthogonal Frequency Division Multiplexing (OFDM) is a basic method for doing high data rates and spectral efficiency requests for wireless communication systems. OFDM transmissions are emerging as important modulation technique because of its ability to safeguard a high level of toughness against any interference [4].

The headway in very large-scale integrated circuits (VLSI) technologies and Software Defined Radio (SDR) offers an answer to implement elastic OFDM systems and channel coding. VLSI is the current level of computer microchip smallness and it refers to microchips holding in the hundreds of thousands of transistors. The development of VLSI equipment has melodramatically impacted the development and improvement of wireless communication systems.

## 2. Related work

In this work is to study the design and synthesis turbo code with OFDM system. Simulation performance of OFDM design in this paper showed successfully result, which composed of the main parts Serial / Parallel, 8QAM, 16IFFT.

System implementation has been done using FPGA technology with Altera Cyclone II boards.

In 2016,prakasita et al presented A model of turbo code encoder based on field programmable gate array (FPGA) for nano satellite application Nano satellite communication schemes are experiential by likening the simulation of image broadcast using nano satellite communication project without channel code, using turbo code with rate of 1/3 and 1/2 , the delay procedure of turbo encoder using 8* 228 bits of interleaver is 11.043 clocks and the maximum frequency of the system was 169.122 MHz .The turbo encoder is applied on FPGA ATLYS Spartan 6 [5] .

Amrutha Jacob and Gopal presented implementation of Orthogonal Frequency Division Multiplexing Transceiver on FPGA , The depended on two types of modulation QAM and PSK. The design was very efficient and it achieved good results [6].

Implementing convolutional encoder by VHDL and simulating by using Xilinx 13.i are presented by Selve and Antony .The encoder design uses constraint length 9 and code rate 1/2 parameters [7].using OFDM modulator and demodulator to generate magic wireless asynchronous transfer

mode (ATM) network are presented by Daniel , this structure which operate in 5 GHz band, is ahead acceptance for OFDM in high rate wireless communications. VHDL will be used for RTL account and FPGA synthesis tools it will be rummage-sale for presentation analysis of the proposed core. Modalism Xilinx edition will be used for verification of results [8] .

An efficient VLSI architecture for turbo encoder and decoder using the convolution interleaver has been designed and implemented by using VHDL with code rate of 1/3 which are obtained by Hegu and Ghodke . this work shows that the VHDL provides lower arithmetic equations and better system performance [9].

OFDM transceiver implementation using FPGA Spartan (3A) kit is presented in [10]. The performance of OFDM system with 64QAM has been simulated using MATLAB toolboxes. The experiment was in three stage, the first to change the length of the FFT/IFFT with fixed SNR, the second stage changes the SNR with fixed FFT/IFFT length and in the third stage, the effect of S/N change is examined over the scatter plot at the demodulator. The best S/N results were obtained at IFFT/FFT length 1024, after this value, there is little effect on the value of S/N .The study of Viterbi algorithm is presented in [11] . Three kinds of models were used in the Branch Metric Unit (BMU) work, Path Metric Unit (PMU) and Surviver Management Unit (SMU) of Viterbi decoder. MATLAB was used in designing and implementing of a convolutional encoder with constraints length of 3 and code rate of 1/2 and Viterbi decoder. When the result are compared with coding and without coding, they show that the coding gain at a specific BER is good.

### 2.1 Turbo Code

Turbo code is one of the most efficient coding systems for FC. The information order is doubled encoded, by an interleaver among the dual encoders portion near type the dual encoded numbers orders about statistically self-governing of both additional. Frequently half rates recursive systematic convolutional (RSC) encoders stay rummage-sale, with each RSC encoder creating a methodical production which stayed equal near the unique data order, along with streamer of parity data. The binary parity commanded could be then compromised before being moved along with the unique information arrangement to the decoder by using puncturing operation. This puncturing of the parity data lets broad domain of coding rates near stayed understood, then frequently half the parity data after every encoder was sent. Fig. 1 showed turbo encoder with a rate of (1/3) [12].

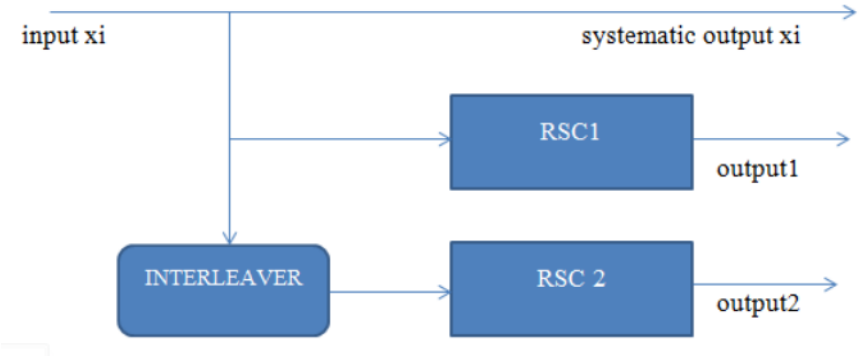



Figure 1: General Turbo code scheme.

The interleaver project has an important effect on code presentation. A little weights code container create poor error presentation, consequently, it is significant that single or together of the coders create codes with decent weight. If an input order (xi) creates a little weight output from RSC1, formerly the interleaved type of xi wants to create a code of decent weight from RSC2. Blocks interleavers offer adequate presentation, nonetheless pseudo random interleavers have been exposed to stretch superior presentation [13]. In this paper used convolutional interleaving. A convolutional interleave contains N rows of shift registers consuming without delay for all row, each next row has

a delay which is R symbols duration progressive than the previous row as shown in Fig. 2. The codeword symbol from the encoder is fed with one code symbol to all rows. With each fresh code word symbol, the observer switches to a new register and the new code symbol is shifted out to the channel [14].

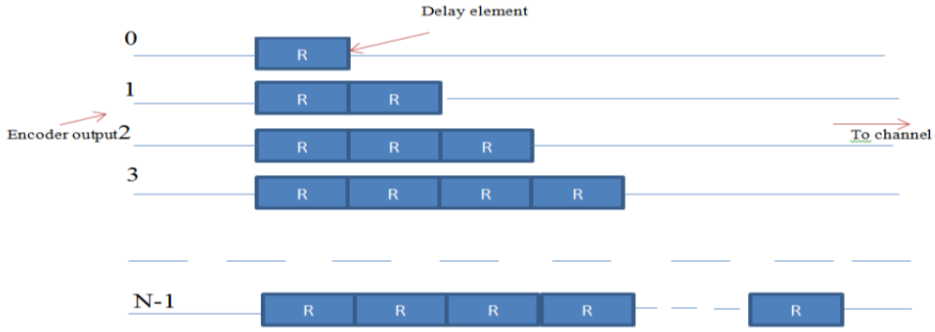
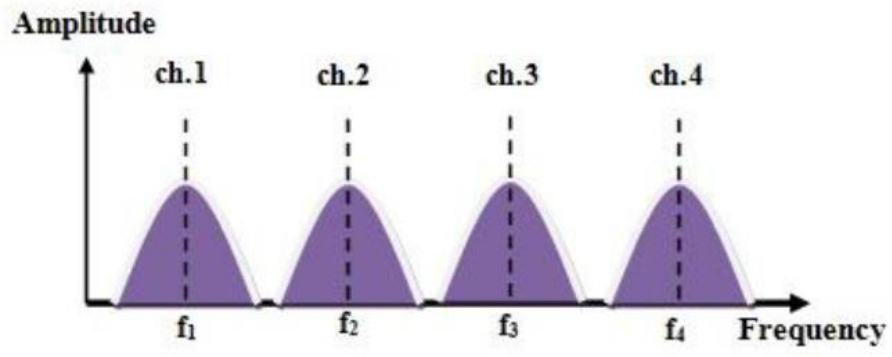


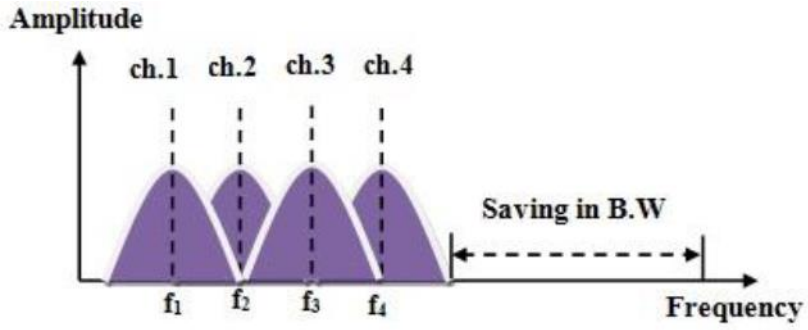

Figure 2: Convolutional interleaves.

**2.2 Orthogonal frequency division multiplexing system.**

OFDM is one of the multi-carrier modulation (MCM) methods that transfer signals over multiple carriers. These carriers (subcarriers) have dissimilar occurrences and they are orthogonal to each other. OFDM systems have been used in both wired (known as Discrete multitone (DMT)) and wireless communications (known as complex transmission) [15]. The OFDM is based on dividing the spectrum available to several sub-perpendicular channels where each narrowband sub-channels skills almost flat fading and letting sub-channels in the frequency domain, thus the transmission rate would increase. This type of modulation is flexible and highly efficient and its ability to prevent inters symbol interference (ISI) by using a kind of embedding with it such as phase shift keying (PSK) or quadrature amplitude modulation (QAM) [16]. Previously, the FDM system used a non-overlapping spectrum and the filters were used to generate the distances between sub-channels. But they were considered as a very inefficient way to provide bandwidth and therefore an OFDM system was created in which the sub-channels were orthogonal at the same time. They provided space in the bandwidth if the spectra of individual sub-channels are permitted to overlap, as shown in Fig. 3. Yet, it is conceivable to place the carriers in an OFDM signal so that the sidebands of the singular carriers overlap and the signals are unmoving without receiving carrier intervention. To ensure this the carrier necessity was arithmetically orthogonal [8, 9].




(a)




(b)

Figure 3: Signal spectrum of multicarrier system, (a) Non-overlapped signal spectrum, (b) Overlapped signal spectrum.

Fig. 4. displays the block diagram of an OFDM transceiver. OFDM signals are made digitally and they contain amount subcarriers that are moderated by PSK or QAM. Later moderating the input data digitally, then the following spectrum is rehabilitated back to its time domain using an Inverse Fast Fourier Transform (IFFT). The IFFT does the transformation very professionally and delivers a simple way of safeguarding the carrier orthogonally [8].

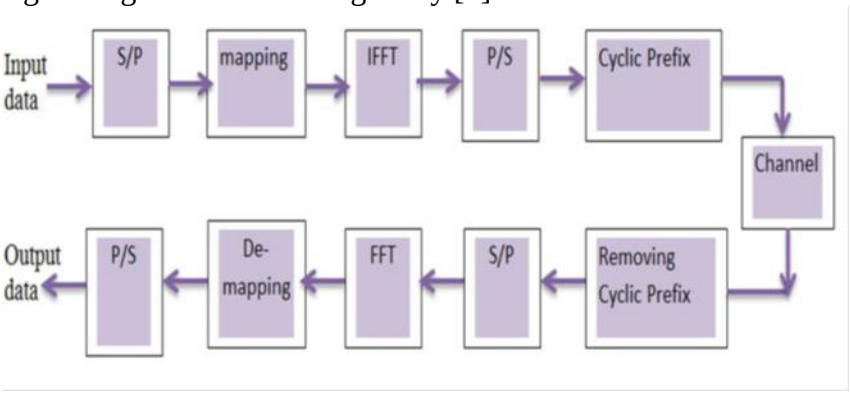



Figure 4: Block diagram of an OFDM transceiver based on FFT/IFFT.

### 3. BER simulation using Matlab

To analyze the performance of the parallel concatenated convolution code (PCCC) and serial concatenated convolution code (SCCC), the Bit Error Rate (BER) has been measured for both of them. To implement of PCCC for different number of iteration (1, 2, 3, 4, 5) with code generator (G) = [3, (7, 5), 7] and block size L = 192 unit is schemed as in Fig. 5. The circuit of PCCC was implemented by using MATLAB and used a binary data source and sent it by an AWGN channel to be recovered from the receiver side by Turbo decoder with the same n and k.

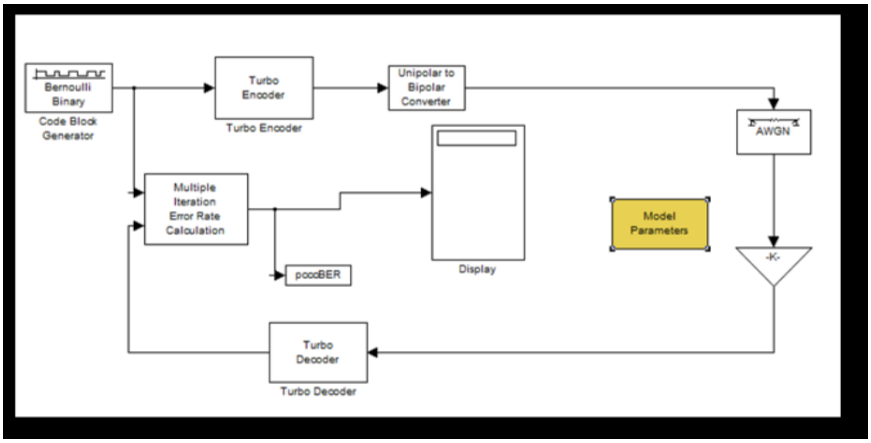



Figure 5: Parallel concatenated convolutional code (PCCC).

Fig. 6. shows the implementation of SCCC for different numbers of iteration (1, 2, 3, 4, 5) with code generator (G) for outer encoder = [3, (7, 5)], inner encoder = [3, (7, 5)] and block size (L) = 192 unit.

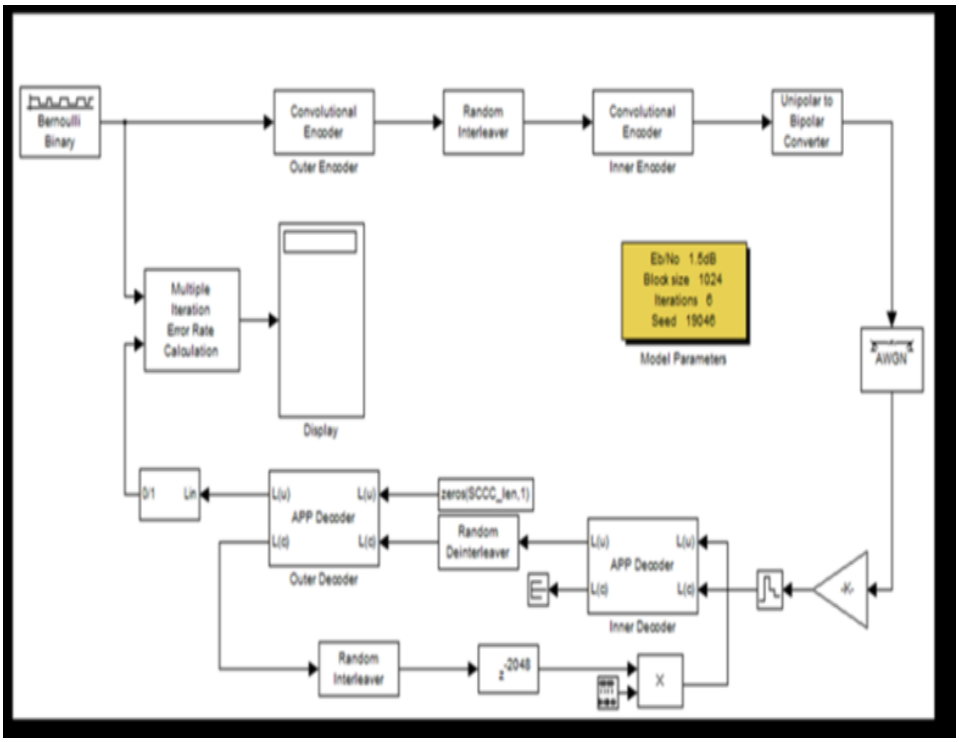



Figure 6: Serial concatenated convolutional code (SCCC).

The above designs results are shown in Fig. 7 and 8. The PCCC is compared with SCCC in terms of the BER with SNR and found that PCCC is more efficient. So that in this work the PCCC is adopted to generate the turbo code.

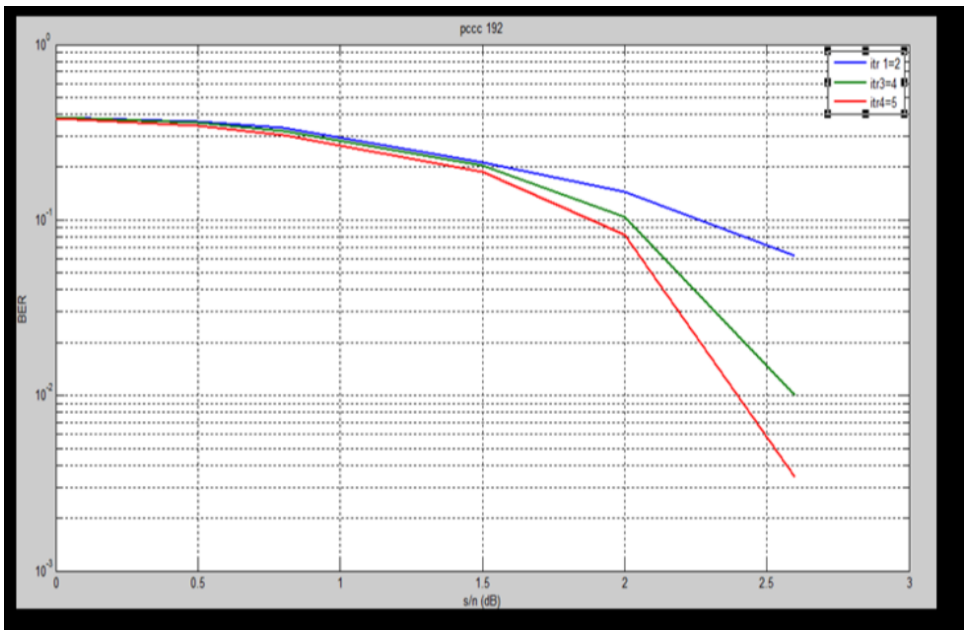



Figure. 7: The relation between BER and S/N (dB) for PCCC.

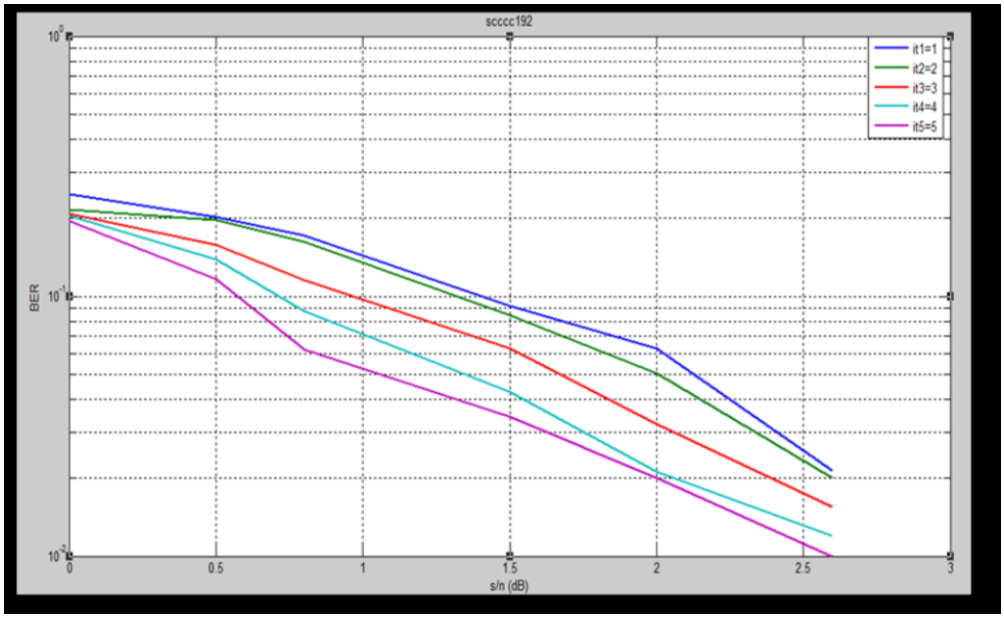


Figure. 8: The relation between BER and S/N (dB) for SCCC.

## 4. Flow chart of the design implementation

The procedure of implementation which is used for typical SDR system was described in Fig. 9. MATLAB (M-file and MATLAB-Simulink) is used for implementing the design as a model and the performance evaluation is performed by functional simulation. When the behavior of the design became persuaded, a VDHL codes will be generated as a next step for the model, also for the simulation purpose, test benches will be generated. The Altera ModelSim tool is used to perform a digital environment to test the behavior of the design once again. Finally, downloading the generated VHDL have been completed on Altera-Cyclone II FPGA-DE2-70 board platform.

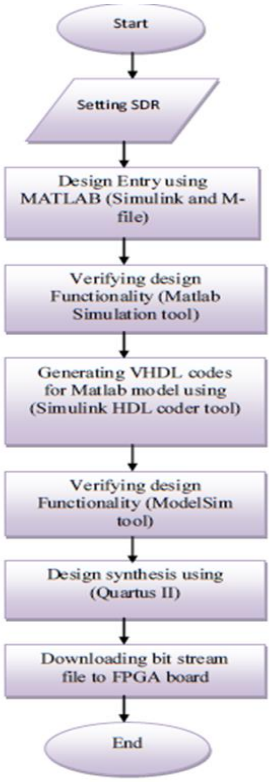


Figure. 9: Flowchart design procedure.

## 5. Turbo encoder with OFDM transmitter implementation

Turbo code contained two convolution codes type RSC and convolutional interleaver based on MATLAB (Simulink and M-file) to satisfy the functionality of the proposed system. However, the Simulink HDL Coder was used to convert to VHDL codes which used to implement a proposed system in FPGA hardware platform. The configuration of the SDR system of the OFDM with turbo encoder is shown in Fig. 10 and performed in a simplest way, where 8QAM and 16IFFT have been selected to implement the OFDM.

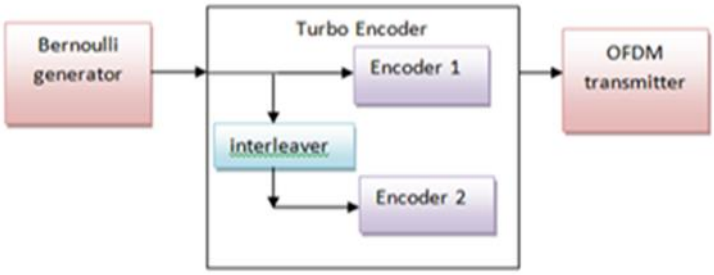



Figure 10: Turbo encoder with OFDM.

The 8QAM has been chosen in this work due to the simplest and least complex of the operation. As the value of M increases, the BER increases and thus the complexity of the system increases. The generators of the encoder were [3, (7, 5), 7] and the interleaver was convolutional interleaver with four rows of shift registers.

The Device Utilization Summary of the OFDM is shown in Table 1.

Table 1: Area summary of the OFDM after synthesis in FPGA

| 8QAM | | 16IFFT | |
|---|---|---|---|
| Type of device | number | Type of device | number |
| AND gate | 9 | AND gate | 7 |
| Mux | 17 | Mux | 240 |
| | | Equal operator | 6 |

Fig. 11 shows the chip planner of the OFDM with turbo code based on FPGA, while Fig. 12 represents the final report of the SDR system for turbo code with OFDM which contained the information around the portions fractions for the implemented SDR system of the FPGA device. It is showed that the total logic element = 283 / 68416 (<1%), total compensational fraction = 248 / 68416 (<1%), dedicated logic registers = 159 / 68416 (< 1%) , total registers =159 and total pins = 21 / 622 (< 3%).

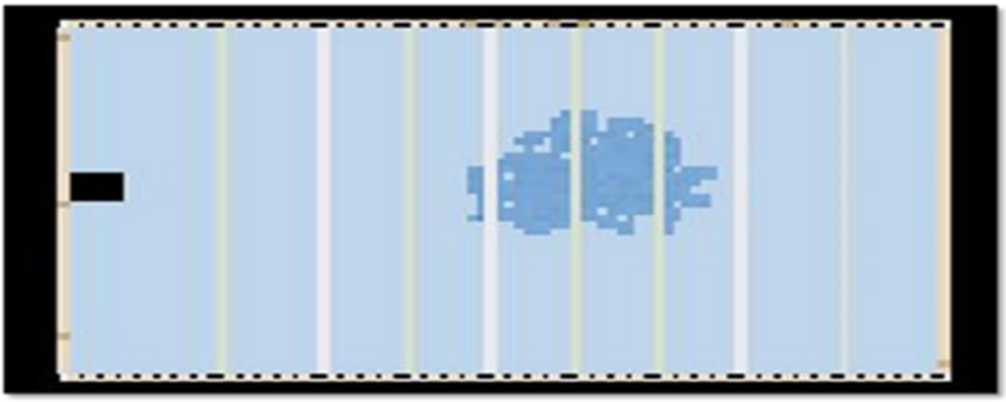


Figure 11: Chip planner of the turbo code with OFDM.

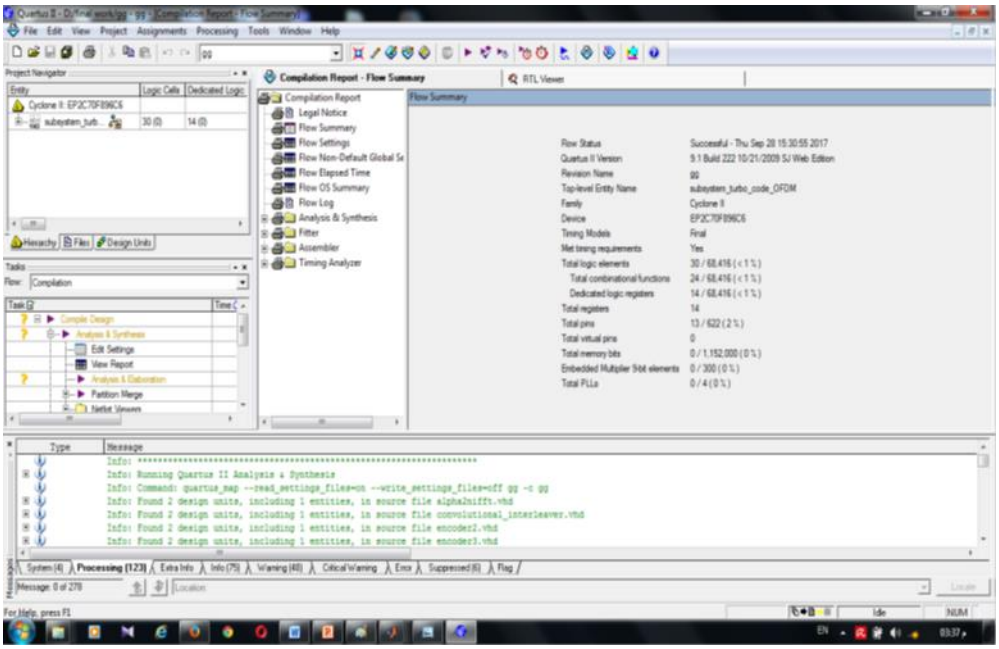


Figure12 : The final report of the turbo code with OFDM implementation

## 6. Simulation results gorithms, codes and listings

Two simulation techniques were used in order to evaluate the performance of the proposed modulator system. The first simulation technique was based on MATLAB version (2012a). The second simulation technique was based on ModelSim. The experimental waveforms were obtained from hardware implementation by using Altera device.

### 6.1 Simulation Results based on Matlab

The simulation based on MATLAB was carried out as the first step in the design and evaluation of the SDR system.

However, the modification in the design could be executed at this stage.

1. Simulation of Turbo code: The Input signal (Bernoulli generator) could be entered to test turbo encoder using two RSCs and convolutional interleaver. Fig. 13 shows the input signal to turbo encoder and three outputs which they represent the same input for output1, RSC1 for output2 and interleave RSC2 for output3. The calculated results show the coincidence with simulation results.

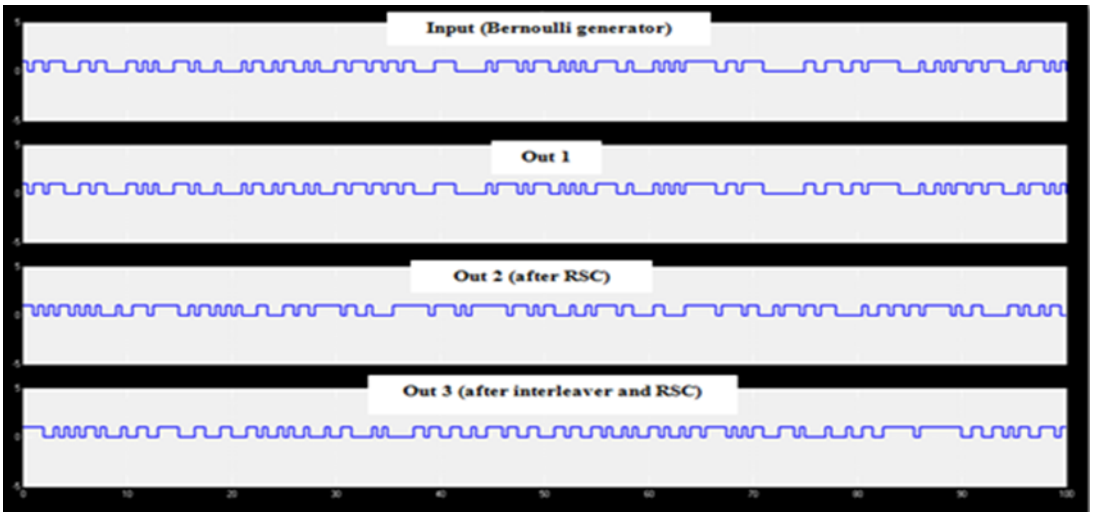



Figure13: Simulation of the input and output signals of the turbo encoder.

2. Simulation of OFDM: Referring to Fig. 4, the Bernoulli Input signal assumed to be the input data for testing the OFDM circuit. Fig. 14 shows the input signal and output for serial to parallel converter, while Fig. 15 shows the output signal of the 8QAM. Fig. 16 shows the output signal of the turbo code with OFDM transmitter.

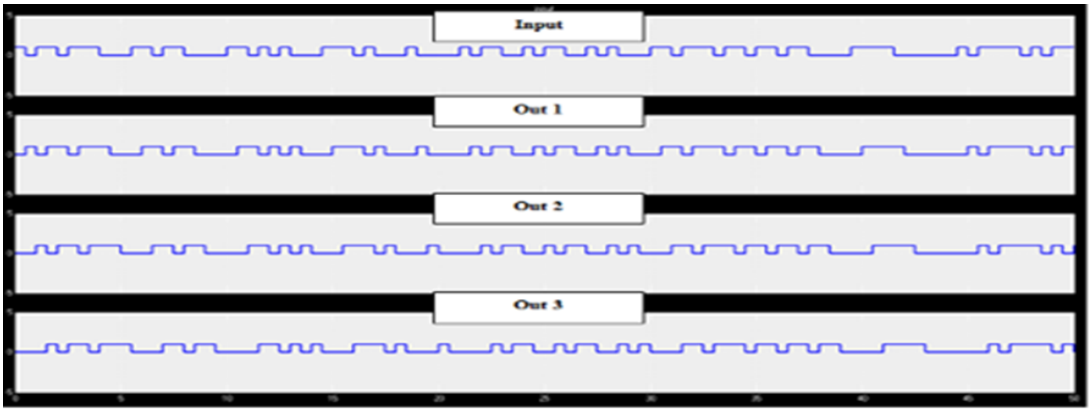



Figure14: Simulation result of the input and output data of the serial to parallel converter

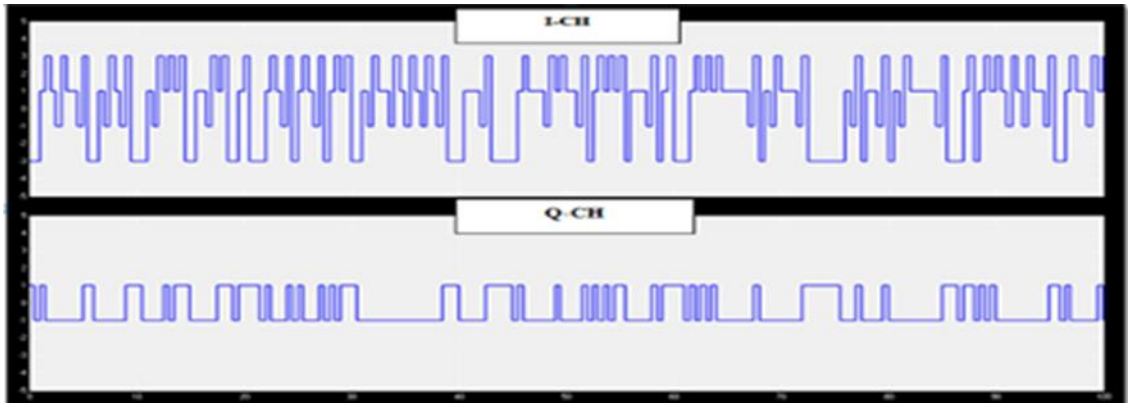



Figure 15: Simulation result of the output signal of the 8QAM.

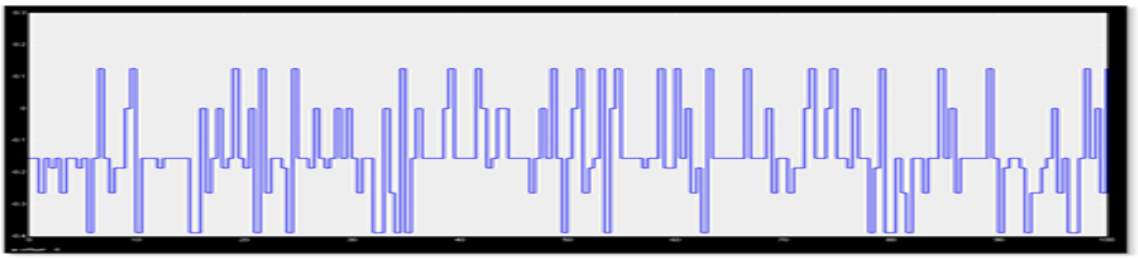


Figure16 :The output signal of the parallel to serial converter.

### 6.2 Simulation results based on Modelsim

ModelSim program was used to test the results of Matlab simulation by using Bernoulli input signal. Fig. 17 shows input and output of Turbo encoder. Fig. 18 shows output signal for parallel to serial converter.

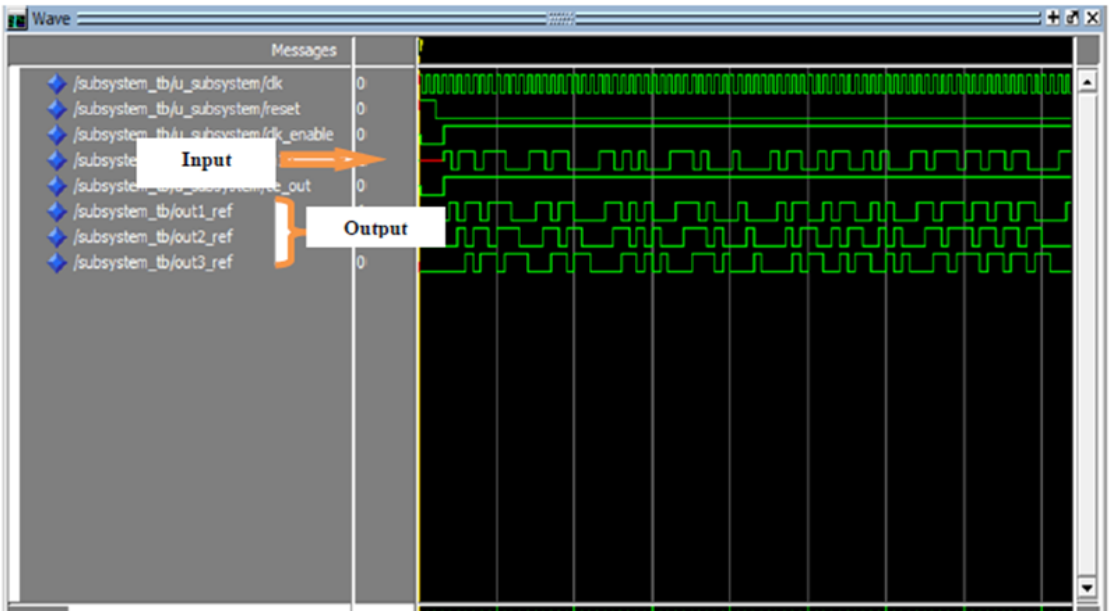



Figure17 : Turbo encoder signals (input and output).

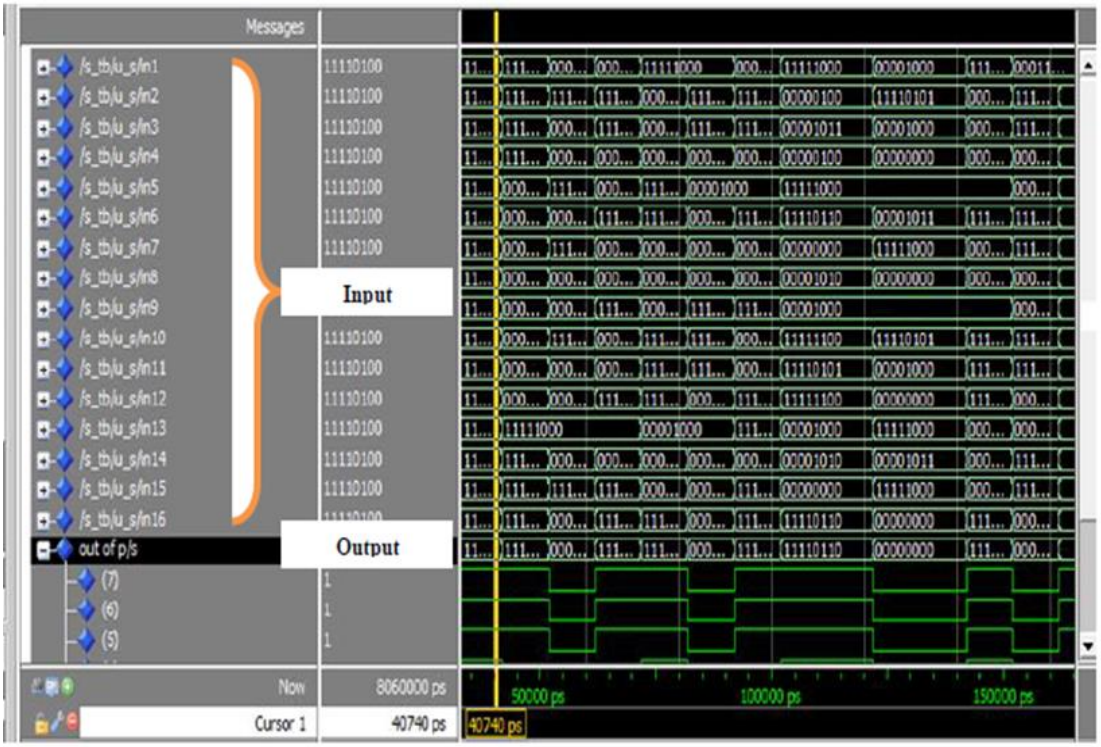



Figure18 : The output signal of the parallel to serial converter.

## 7. Experimantal results

After compiling the VHDL code by using Quartus II and downloading the bit streams successfully to Cyclone II FPGA family, Altera DE2 kit. Square wave signal from function generater has been applied as the input to the kit, while the output has been measured by an oscilloscope. Fig. 19 represents the practical connection of system. Fig. 20 appears the output data for (16IFFT) with turbo encoder at frequency =100 KHz.

Figure. 19. Practical connection of system for transmissions.


Fig. 20. The output signal for transmission at F=100 KHz.

## 8. Conclusions

The design and implementation of the SDR proposed system based on HDL Simulink Coder give more flexibility and more confidence because of the ability to examine the system performance at any point in the design process. Two simulation steps are used in the design process to examine the system performance according to the required system specification and the target platform used to implement the proposed system. The first step is the MATLAB simulation tool gives the designer a clear view of the system parameters required to complete the design. The waveforms at any point in the system can easily be obtained and it is necessary for checking the system functionality and the second step is Modelsim environment tool gives a complete HDL simulation environment to test the functionality of the VHDL code for the SDR proposed system. VHDL code functionality is applied successfully to all designs proposed in this work. The research survey concluded that because the number of users did not increase, the capacity of the channel should be increased so that there could be an opportunity for increased noise and would affect the channel's bit error rate. Therefore, there should be a need to provide reliable data transfer by improving the bit error rate of the Turbo code used in most real-world applications. This can be done by a device such as FPGA to encode data more efficiently and faster. The simulation results of the MATLAB and Modalism show the coincidence between them.

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